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—REVIEWS—

Silicon-On-Insulator by Wafer Bonding: A Review

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ABSTRACT

Various approaches to wafer bonding technology are reviewed. Bonding kinetics are discussed as well as different mechanical and chemical thinning techniques. The structural and electrical qualities of state-of-the-art bonded SOI silicon films and devices built in them are detailed. Problems faced by this technology are evaluated.

Silicon device isolation by wafer-to-wafer bonding without any glue layer has been known for more than a quarter of a century, since Kenney applied for a United States patent in 1964 (1) (although the bonding process he used was meant to only transfer the device layer, rather than provide a semiconducting substrate). The bonding was assisted by very high temperature, 1225°C, and pressure, 2000 psi. A somewhat less cumbersome technique was introduced by Wallis and Pomerantz (2) for bonding silicon wafer to fused quartz, and investigated for silicon-on-insulator (SOI) applications by Anthony (3) and Frye *et al.* (4). This technique used lower temperatures, 850°-950°C (2, 3), and an externally applied electric field, which replaces hydrostatic pressure in providing the pulling force needed to achieve intimate contact of the wafer surfaces. The applied voltages ranged from 20 to 50V (3, 4). The major drawback of the field-assisted techniques is the need for electrical contact to the wafers at high temperature, making the process incompatible with batch processing and prone to contamination.

The potential of the wafer bonding technique became widely recognized after the first reports of SOI substrates produced by bonding without an externally applied electric field or pressure were published in 1985-1986 by Lasky *et al.* (5-7) and Shimbo *et al.* (7). The bonding process, followed by the removal of most of one of the wafers by mechanical and/or chemical means, creates a generic (nonmask-specific) SOI wafer. This technique provides an insulating oxide and a high-quality silicon device layer (comparable to bulk), as well as thermal oxide interfaces between the buried SiO_2, the device layer, and the silicon substrate. It inherently permits the use of a wide range of thicknesses of both the insulating oxide and the device layer, which allows for more design flexibility. Applications, including pressure sensors (8), improved dielectric isolation (DI) wafers (9), complimentary metal-oxide-semiconductor (CMOS) transistors in a very thin (30 nm) silicon film (10), and 256 K static random access memory (SRAMs) (11), have been reported.

In this paper we review and discuss various aspects of wafer-bonding SOI technology and summarize the status of the art.

Process Steps

The SOI wafer is created in four basic process steps: (i) Formation of an etchstop (by implantation or epitaxy) or polish-stop (an imbeded grid of slow polishing material, *e.g.*, SiO_2) in one of the wafers (the seed wafer). In the case of a nonselective polish-back approach, a plain oxidized wafer is used. (ii) Contacting the polished face of the seed wafer with that of another wafer (the handle wafer), oxidized or not, in ambient temperature and atmosphere. (iii) Bonding the pair at an elevated temperature. (iv) Grinding and etching or lapping and polishing the pair from the seed wafer side to the desired thickness of the silicon device layer.

Room Temperature Bond (Contacting)

Two flat, smooth, hydrophilic surfaces can be bonded at room temperature (or "contacted") without using external force. The bonded materials can be metallic, semiconducting, or insulating in nature. The contacting forces are believed to be caused by attraction between hydroxyl groups (—OH) (5, 7, 10, 11) and possibly some water molecules (13, 14) adsorbed on the two surfaces. The attraction can be significant enough to cause the spontaneous formation of hydrogen bonds across the gap between two wafers. The spontaneity in the initiation of the contacting occurs only between exceptionally flat, smooth, and clean surfaces. Once initiated, this bonding process can spread in a form of "contacting wave" throughout the entire area between two Si wafers with speeds of several cm/s (10, 14).

The hydroxyl groups are usually attached to the surface through the reaction of a clean surface oxide with the moisture from the air or atomized water source. Numerous other surface treatments can be used, if needed, to improve the hydrophilic properties of oxide surface. Ammonium hydroxide soaks (4, 10), sulfuric acid (7), NH_3 plasma (15), and other treatments (16, 17) were proposed. After treatment, the wafers are usually washed in DI water and dried in N_2 at room temperature before contacting.

Bonding

Although room temperature bonds can withstand grinding and etchback processes (18), it is customary to strengthen the bonds by annealing at temperatures ≥800°C.

Kinetics of bonding have been extensively investigated for temperatures ranging from 20 to 1400°C, and times from 10s to 6h (10, 12). The bond strength was measured in terms of surface energy γ by a technique based on the theory of crack propagation in linear elastic solids (10). The energy is plotted *vs.* bonding temperature in Fig. 1 for a bonding time of 10 min.

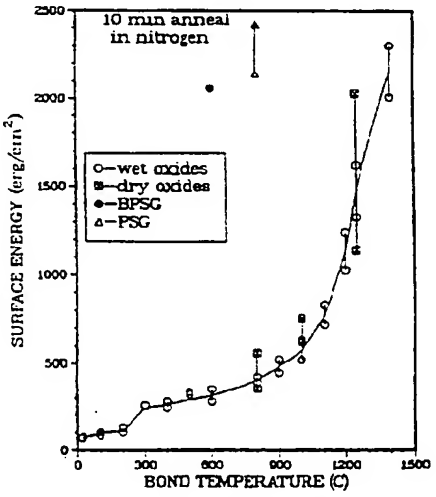


Fig. 1. Surface energy vs. bonding temperature for bonds between wet oxides 300 nm thick (3 in. Si wafers). Also shown are energies for dry oxides (3 in. wafers), BPSG (4 in.), and PSG (4 in.).

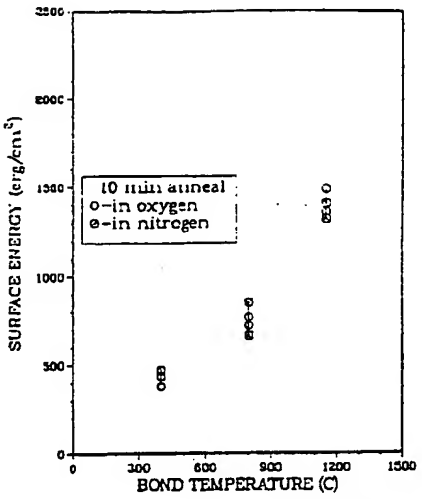


Fig. 2. Surface energy vs. bonding temperature; 4 in. wafers with wet 300 nm thick oxide bonded in N_2 and O_2.

The bond strength increases monotonically with temperature and exhibits three distinct phases. The first phase, hydrogen bonding between hydroxyl groups (OH) on one surface with the oxygen atoms of either the SiO_2 or OH groups on the other, begins at room temperature and starts being replaced by the second phase, the Si—O—Si bond, around 300°C. This phase involves elastic deformation of the wafers in the locally unbonded microareas and dominates through temperatures up to about 1100°C. Finally, in the third phase, viscous flow of the oxide around and above 1100°C leads to complete bonding. The surface energies of bonds between dry oxidized wafers are similar to those of bonds between oxides grown in steam.

Several researchers have chosen bonding in an oxygen atmosphere, explicitly (6) or implicitly (15, 23), indicating that it produces bonds superior to those formed in nitrogen gas. It is rather unlikely that, for the times and temperatures used in typical bonding, oxygen gas can diffuse through the crack, at best one or two monolayers wide, for distances comparable to the radius of the wafer. We have conducted an experiment to test this hypothesis. Figure 2 shows bond strengths measured for the oxidized (300 nm thick oxide) 4 in. wafers contacted in air and bonded in dry oxygen or nitrogen, respectively. Temperatures of 400°, 800°, and 1150°C were used. There is no difference, within experimental error, between bond strengths corresponding to the two bonding ambients.

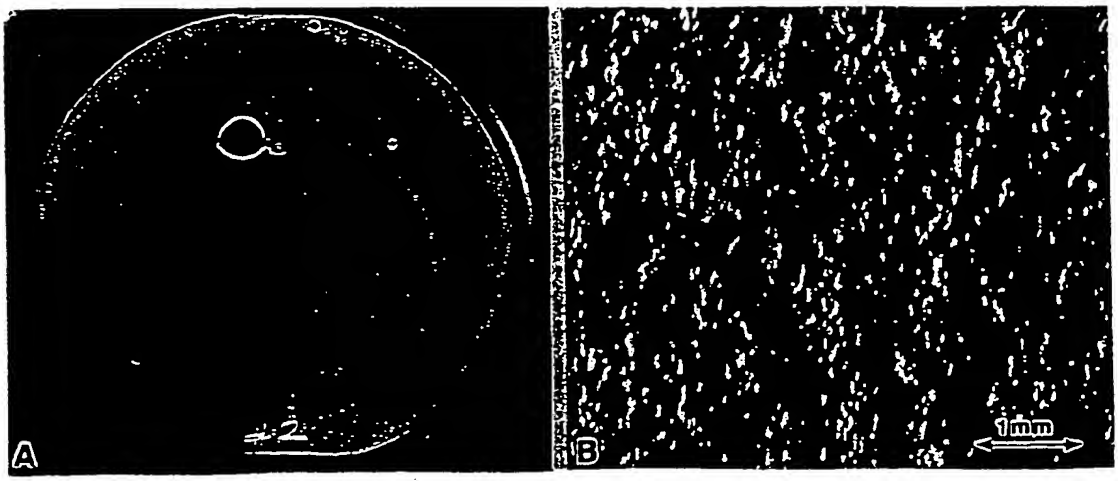
Wafer Parameters vs. Bonding

It should be noted that although the model discussed above describes the general kinetics of wafer bonding, the values of the surface energies observed in our experiments represent only those particular sets of wafers tested. In accordance with the model, higher densities of ≡Si—OH groups, smoother and more planar surfaces, lower softening points of the oxides, or thinner wafers, will all contribute to a stronger bond, i.e., parts of or the whole γ vs. temperature curve will shift toward the lower temperatures. The effect of these properties on bonding will be briefly discussed below. It was an inadequate quantity of any of the above parameters that forced earlier researchers to facilitate bonding with the assistance of an external force (hydrostatic pressure, electric field).

Hydrophilic surfaces.—Stengl *et al.* (14) measured the speed of the contacting wave between two silicon wafers at different temperatures and found it to decrease monotonically to zero as the temperature increased to 320°C. This reflects the loss of the source of the attractive force, presumably due to the thermal decomposition of the silanol group and desorption of the freed OH group.

Surface roughness and flatness.—The range and strength of the hydrogen bond forces are sufficient to elastically deform wafers, whose macroscopic flatness deviates over many micrometers, to achieve conformity of the two surfaces in room temperature bonding. The deformation also happens microscopically, accommodating some of the surface roughness. Both types of deformation are illustrated in the x-ray transmission topographs of the bond in Fig. 3. The change of the x-ray image contrast reflects the strain in the lattice due to the global (Fig. 3a) and local (Fig. 3b) deformations. The "roughness" of the latter has a spatial wavelength on the order of 0.1-1 mm. The areas at the edge of the wafer and in the large void of Fig. 3a that were not bonded exhibit smooth appearance indicating lack of local strain clearly in support of the postulated bonding-caused deformation. The roughness imaged by the x-ray topography does not appreciably change in the temperature range up to 1200°C, indicating that most of the deformation of the wafers happens during contacting.

In light of the above discussion, one should expect that wafers with a rougher surface, which require more deformation to conform to each other, should produce weaker bonds at a given temperature, all other conditions kept equal. The microroughness of a thin film surface would depend on both the original wafer surface topography and the film formation process. In particular, the roughness of



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the insulating layers (thermally grown or deposited) utilized in the wafer-bonding SOI wafers affects their bond strength.

Thermal oxides.—Thermal oxides are very smooth and, unlike most of the deposited films, their microroughness is not detectable by stylus profilometry or Nomarsky optical microscopy. Hahn *et al.* (20) have found, using light scattering and low energy electron diffraction (LEED) methods, that the roughness of silicon surface increases with the thickness of SiO_2 layer grown on it (for a given growth temperature). We reason then that the oxide surface should also become rougher with the increasing thickness, at least for some small thicknesses, where the topography of the oxide surface can be affected by the local SiO_2 volume changes at the growth (i.e., Si—SiO_2) interface. It would be expected, then, that at least for thin oxides, the bond strength would decrease with increasing thickness of the thermal oxides of bonded wafers.

Silicon wafers with oxides of different thicknesses, all grown in steam at 850°C, were bonded in pairs and their surface energy measured. Figure 4a shows two surface energy *vs.* oxide thickness curves for wafers bonded at 800° and 1200°C, respectively. Both curves exhibit a rapid decrease of surface energy with increasing oxide thickness for thicknesses up to 200 nm. The energies for the wafers with 1-2 nm thick (native) oxides were unmeasurable, because the bonds were so strong that the wafers cracked upon the insertion of a blade used in the energy measurement technique. The curve for the 800°C bond levels off for oxides thicker than about 200 nm. Both the initial drop-off of the energy and its subsequent leveling off are in accordance with the postulated change of the oxide surface roughness. We believe that the increase in surface energy (after the initial drop-off) with increasing oxide thickness for the samples bonded at 1200°C is caused by easier oxide flow in the thicker oxides at that temperature.

An attempt was made to verify the model by evaluating the roughness of the five oxides used in the above bonding experiment. Long, linear scans of the surface profile with a stylus profilometer (60 μm scan) and an optical profilometer (660 μm scan) were used, as well as local two-dimensional (1 × 1 μm) scans with two different atomic force microscopes (AFM) to assess the roughness. Figure 4b shows the relationship between the root-mean-square (rms) roughness of the thermal oxide surfaces and their thickness as measured by the four instruments. The scatter of the data from sample to sample, as well as for any given sample (the latter partially caused by the difference in the scan size), is too large to draw any conclusions in support or against the proposed model. The main reason for the inconsistency is believed to be the very high level of smoothness of the samples, comparable to the resolution limit of the measurement technique.

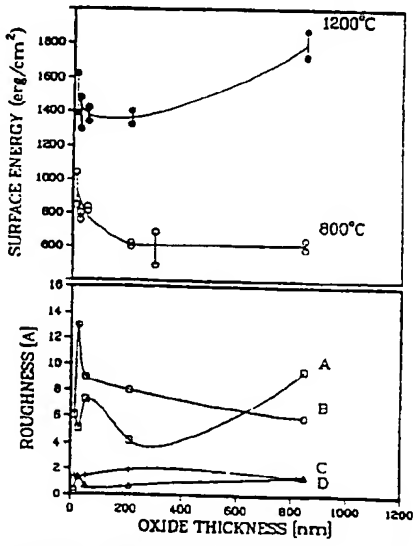

Fig. 4. (a) Surface energy *vs.* wet oxide thickness after bonding at 800° and 1200°C, (b) surface roughness (rms) *vs.* wet oxide thickness by optical (curve A) and stylus (B) profilometry, and 2-D imaging with two different atomic force microscopes (C and D).

Deposited films.—The chemical vapor deposited (CVD) films are usually rough and fail to contact and bond to even very smooth silicon wafer surfaces without an externally applied force. Smoothing the surface by chemomechanically polishing the hard (undoped) oxides or annealing (flowing) soft (phosphosilicate [PSG] or borophosphosilicate glasses [BPSG]) oxides significantly improves their bonding capability. In particular, annealing previously nonadhering wafers, covered with a BPSG (4% of B, 4% of P) film, at 950°C for 15 min caused the two wafers to subsequently bond very well. Also, because of the lower viscosity of the BPSG, bonding was completed at lower temperatures. A 600°C, 10 min process was sufficient to increase the bond strength about sixfold over that measured for two thermal oxides bonded at the same temperature. PSG films showed similar performance (Fig. 1). If the high content of boron or phosphorus in those films can be ignored (*e.g.*, in some sensor applications) or dealt with (using diffusion barriers such as Si_3N_4), these glasses can be used as adhesion layers when wafer bonding at low temperatures is required.

Wafer thickness.—Thicker wafers, being stiffer, are expected to yield less to the local pulling forces of the bonds forming across the gap between them. A weaker bond should result in bonding at a given temperature. It has been shown that thinner (more flexible) wafers bonded more strongly at a given temperature (10). The practical aspect of this phenomenon is that due to the very high flexibility of a seed wafer after it is thinned to about 1 μm or so for SOI applications, normal processing temperatures should suffice to further increase bond strengths.

We have found that, contrary to the above, the bond strength for 4 in. wafers was consistently higher than that for the 3 in. ones, although the latter are thinner. A possible explanation is that the surface smoothness of the larger wafers is sufficiently better to offset the disadvantage of their increased thickness.

Voids

The single most important problem faced by bonding technology is the lack of local bonding, leading to delamination and subsequent loss of the device film in the unbonded region. Two types of voids can be discerned: "extrinsic," formed during the contacting process, and "intrinsic," which are generated at elevated temperatures.

Particulate contamination or, more rarely, other residue present on the surface of either wafer is responsible for the former. An extreme lack of flatness and/or poor local hydrophilization of the surface may also lead to void formation. The voids are formed when the advancing contact wave surrounds the contaminated area, trapping ambient gas in it. For a given size of particle, the thicker (stiffer) the wafer, the larger the void will become. On might expect that the oxygen gas trapped in the void during contacting would be locally consumed by chemical reaction of the Si—O—Si bond formation, or outdiffusion into the two substrates during bonding at elevated temperatures. This in turn would lead to the collapse and rebonding of the void. We have not observed any appreciable void reduction. The change in the void sizes in the wafers annealed up to 1100°C for 30 min is negligible (some slightly increase or decrease) for pairs contacted in air or oxygen. Similar findings for the samples contacted in air, oxygen, and vacuum were reported by Black *et al.* (21) and for samples contacted in air by Stengl *et al.* (17). Much of the particulate contamination is of organic origin and it is likely that upon its decomposition at higher temperatures reaction products interact with the void surface, rendering it unbondable. We have seen a condensation-like decoration of some voids in bonded quartz-silicon wafer pairs,

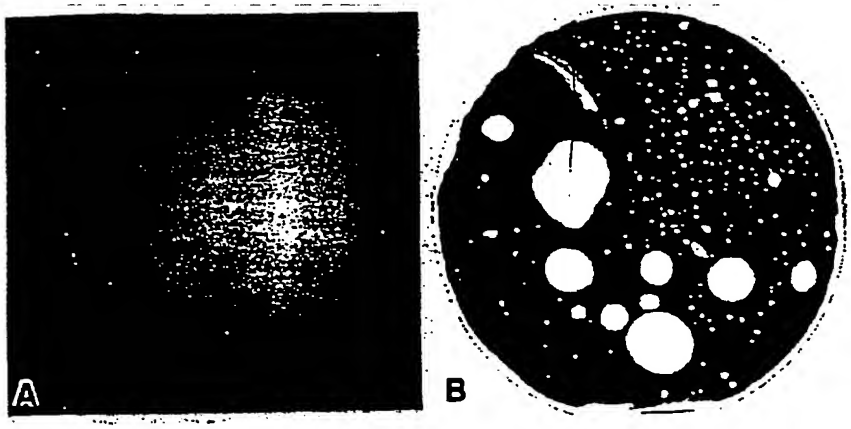

Fig. 5. Bonded 4 in. wafers imaged with: (a) infrared, and (b) ultrasound.

Intrinsic voids can be generated at elevated temperatures. Ohashi *et al.* (9) has reported void generation at and above 200°C, followed by disappearance of the voids around 700°-800°C for wafers with native oxides. Similar behavior has been observed by Bengtsson and Engstrom (22) and Lehmann (23). No such voids were reported for thermal oxide bonds. Outgassing of hydrocarbons adsorbed at the wafer surface has been proposed as the cause of these voids (23). Thermally-generated voids in bonded sputtered oxides were also observed (24). In this case gas incorporated into the film during sputtering outgassed during bonding. Void generation was strongly suppressed by annealing sputtered films prior to bonding.

Voids can be visualized by a variety of methods. The bond between silicon wafers can be analyzed by infrared (IR), ultrasonic, or x-ray imaging, or by thinning one of the wafers down to its oxide layer to visually inspect the voids. In the last case, the majority of voids bulge up due to the release of the compressive stress stored in the oxide film, thus becoming more visible. Visible and IR imaging are based on interference effects and thus are limited to voids whose height is more than about 1/4 of the probing wavelength. IR imagers are the most convenient real-time observation tools and can register voids of about 1 mm diam and bigger. X-ray topography (XRT) has the best resolution, tens of micrometers, but is very time consuming (several hours for a 4 in. wafer) and expensive. Reflection ultrasonic imaging relies on the enhancement of the beam energy due to reflections off imperfections at the bond and is found to produce somewhat more detailed images than IR. The image formation, however, takes much longer. Figure 5 shows a side-by-side comparison of full wafer images obtained by IR and ultrasonic methods. Many small voids seen in the latter do not appear in the former. The images in Fig. 6, formed by ultrasound, XRT, and optically (after full etchback), and magnified by factor of about two, show the capability of these methods for imaging small voids.

An external force, hydrostatic or electric, can somewhat remedy the lack of local bond formation in an inferior wafer pair by forcing the opposing surfaces of a void into intimate contact at elevated temperatures (21, 25, 26), particularly when the void is located near the wafer edge and can vent entrapped gas.

Stengl *et al.* (17) introduced a promising concept of water jet cleaning of two wafers in close proximity, which does not require a clean-room environment and contributes to a dramatic reduction of voids.

Device Layer Formation

The bonding process is followed by thinning of one of the wafers (the seed wafer) to an appropriate device film thickness. The diagram in Fig. 7 shows various thinning techniques utilized in SOI wafer formation. Two basic approaches have been used. The first is lapping (or grinding) and chemomechanical polishing, and the second, grinding followed by selective etchback (the, so-called, BESOI technique [bonding-and-etchback SOI]). The grinding is primarily a rather crude, time-saving step that can be used to remove all but the last several tens of micrometers of the seed wafer. The polish-back with no polish-stop thinning technique is an excellent choice for thick (>1 μm of Si) SOI applications such as bipolar analog circuits, BiCMOS, high-voltage, high-power, or micromechanical sensors. The etchback with double etchstop formed by B^+ implant and epitaxy, or by double epitaxial layer (p^{++} epi and device epi), seems to be the best approach so far for thin-film (<0.5 of Si) SOI. A summary of the parameters for all the thinning techniques is given in Table I.

The polish-back process.—The standard polishing method is cheaper than the etchback technique but the thickness uniformity of the device layer is limited by the flatness and parallelism of the handle wafer (the SOI substrate).

A modified version of this thinning method employs a polish-stop layer consisting of a pattern made out of a slow

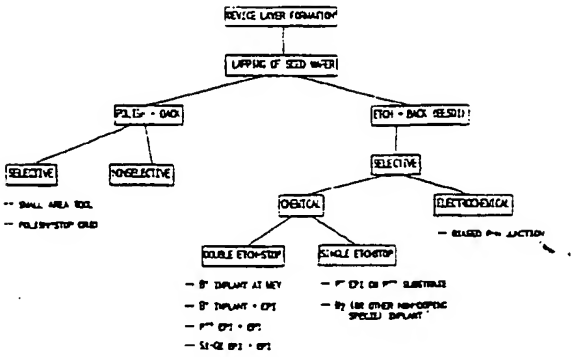

Fig. 7. Thinning techniques for SOI by wafer bonding

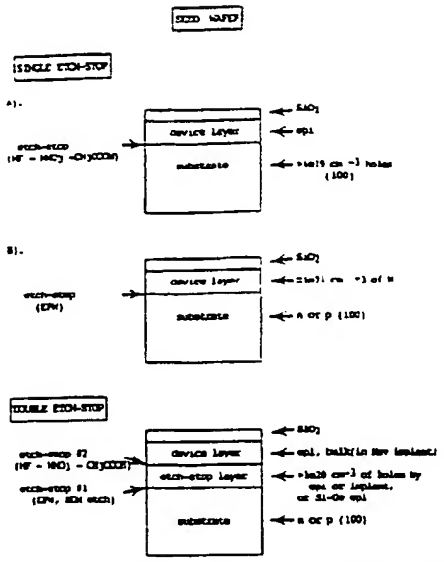

Fig. 8. Seed wafer structure for various etchback thinning techniques

polishing material such as SiO_2 buried in the device wafer (28). It is mask-specific and more complex than the no-stop polishing, but can produce layers with much better thickness uniformity.

Another polishing technique has been proposed by Yamada *et al.* (29). Here, local polishing with a small-area tool was combined with thickness mapping in a computer feedback loop. This method seems to have the best potential to produce cheap, generic SOI wafers with highly uniform silicon films for CMOS as well as other, less-demanding applications.

The etchback process.—After initial grinding, the remainder of the seed wafer is further thinned by chemical or electrochemical etching. A built-in etchstop is used to reduce the etch rate by several orders of magnitude. Figure 8 shows the structure of the seed wafer for various etchback techniques.

The selective chemical etchback thinning technique has two basic variants: a single or double etchstop. The first involves the selective removal of a p^{++} wafer with an HF-based etchant that leaves behind a low-doped epi device film. The etchant is usually a mixture of HF, HNO_3, and CH_3COOH in the ratio of 1:3:8 (the 1-3-8 etch) (30). The limited selectivity allowed by this technique results in only moderate silicon film thickness uniformity. Moreover, the etch requires electrochemical control of the oxidizer content to maintain its selectivity (18). The etch abruptly reduces its etch rate upon reaching highly resistive material and produces a passivation layer, a porous SiO_x that can be as thick as 70 nm. This layer can be removed by a mixture of HF and an oxidizer such as HNO_3, $KMnO_4$, etc.

The double etchstop technique requires a buried p^{++} layer in a low-doped wafer. This structure can be created by implantation of boron alone, or an implant of boron followed by the growth of a low-doped epi film on the seed wafer before bonding (10). In the first case, a high-energy (>1 MeV) implant is required to obtain a device layer with an appropriate carrier concentration ($<1e16\ cm^{-3}$). We were also successful in utilizing a double-epi procedure (p^{++}, p^-) which simplifies the technology and avoids a certain amount of surface roughness related to the p^{++} implant damage. Two selective etches are used to remove the p^- wafer and p^{++} buried layer, respectively. An ethylenediamine-pyrocatechol-water (EPW) etch (31) is used to remove most of the remainder of the low-doped seed wafer. A 1-3-8 etch removes the p^{++} layer. The combined selectivity of the etches is greater than 10,000:1. The final thickness uniformity in this as well as the single etchstop approach depends on the uniformity of the last etchstop

Table I. Summary of wafer thinning techniques for the wafer-bonding SOI, current best results

Method of thinning	Si thickness uniformity (μm)	Roughness	Process complexity	Comments	Reference
Polish-back					
1. Regular	±0.2	Excellent	Low	Si thickness uniformity depends on handle wafer	(27)
2. Small-area tool	±0.4	Excellent	Mod	Si thickness uniformity is independent of handle wafer	(29)
3. Polish-stop	±0.02	Excellent	High	Mask specific, complex	(28)
Etchback					
Chemical					
1. Single etchstop					
a) p^- epi on p^{++} substrate	±0.03-0.07	Good	Low	Difficult etching	(5, 25)
b) N_2 implant into p or or n substrate	±0.002	?	Low	Implant damage (?) High N_2 content	(32)
2. Double etchstop					
a) B^+ implant + p^- epi	±0.005	Very good	Mod	Etchpits $\leq 10^3/cm^2$	(This work)
b) p^{++} epi + p^- epi	±0.012	Excellent	Low	Etchpits $\leq 3 \times 10^3/cm^2$	(This work)
c) B^+ implant at MeV	±0.005	Excellent	Low	Expensive implant	(Unpublished)
d) Si-Ge epi + p^- or n^- epi	±0.02[a]	?		MBE growth, misfit dislocations	(34)
Electrochemical					
1. Biased p-n junction etchstop	Good[b]	Poor	High	Complex preparation for biasing	(18)

[a] With diamond machining.
[b] 200:1 selectivity.

plane distance from the original surface of the seed wafer, i.e., the top epi thickness and/or boron implant uniformity. The increased total selectivity of the etchback process, in conjunction with a very good epi deposition source, recently produced silicon film thickness uniformity with an average standard deviation $\sigma = 12$ nm for double-epi SOI wafers, and $\sigma = 4$ nm for the single-epi ones, across a 4 in. wafer.

A successful attempt to create a buried etchstop by N_2 implantation (32) has been recently reported. A nitrogen dose of 4e16 cm^{-2} implanted at 120 keV was found sufficient to significantly reduce the etch rate of the EPW etch. Annealing at high temperatures had little effect on the etch rates. A similar successful etch-stopping property of implanted carbon has been reported by Lehmann (33). It is not clear at this point what causes the etch-stopping action here. Neither the nitrogen nor the carbon implant provides the carrier concentration available in the activated boron etchstop implant. Nor is the concentration of the species high enough to form a continuous stoichiometric Si_3N_4 or SiC layer that would dramatically alter the EPW etch rate. The quality of the Si films remains to be assessed. Substantial amount of implant damage and implanted species-related precipitation is likely to be present in the film, and an extensive thermal treatment may be required to alleviate these deficiencies. However, the reported Si layer thickness variation of less than 2 nm across the nitrogen-implanted wafer is very impressive and certainly invites further investigation of this technique.

A molecular beam epitaxial (MBE) grown $Si_{0.7}Ge_{0.3}$ layer has been investigated as an etchstop layer by Godby *et al.* (34). Low etch selectivity (17:1), the expense of the MBE process, and misfit dislocations (although mostly confined to the etchstop these may lead to an imprint of their pattern on the device layer after the etchback) are drawbacks associated with this technique.

An electrochemical etchback has been proposed where a reverse-biased p-n junction serves as an etchstop (18). The junction is created by an n-type epilayer deposited on a low-doped p substrate. KOH-based etch is used for the etchback. An elaborate wafer preparation scheme to provide bias through the SOI oxide, and a final orange-peel type of roughness, renders this technique less attractive than the others described above.

Bonded Wafer SOI Properties

Structural properties.—SOI wafers produced by bonding and thinning have thermally grown insulating oxide and Si film-SiO_2 interfaces. There are no traces of a bond in the SOI oxide in fully processed wafers (10). Etch pit densities in the films produced by the etchback of single-epi + boron implant seed wafers were reported below 1000/cm^2 (10, 19). We have obtained counts below 300/cm^2 for the double-epi seed wafers. This suggests that the residual implant damage may not be the sole factor contributing to the defects as proposed earlier (10). The epi growth process is another likely source of some of the observed imperfections. There are no reports, to our knowledge, of defect densities in polish-back wafers, although one would expect them to be very low, comparable to the bulk wafers. No defects were observed in the Si films of BESOI wafers by cross-sectional transmission electron microscopy (TEM).

Silicon layer thickness uniformity, as mentioned above, varies from ± 0.2 μm for the best generic polish-back wafers to about ± 0.004 μm for the ones obtained through the double etchstop procedure. Wafer warpage was comparable to the source material (<15 μm bow in 4 in. wafer).

Roughness of the top surface of the silicon film is difficult to assess quantitatively for these fine surfaces, although it can be discriminated with the help of Nomarsky optical microscopy. The double-etchstop samples with a boron implant are slightly rougher than the ones with a double-epi structure. Those in turn are minimally less smooth than the polished surfaces. However, high-resolution TEM observations could not distinguish among these surfaces.

Table II. Hall mobilities and carrier generation lifetimes in the wafer-bonding SOI films

Mobility (cm^2/Vs)		Carrier lifetime (μs)	Reference
Electrons	Holes		
		15-20	Maszara *et al.* (10)
		27	Lasky *et al.* (5)
	350		Spangler and Wise (35)
1096	409		Xu *et al.* (16)
(1160)	(420)		Xu *et al.* (16)

Control bulk data in parentheses.

method (10) and was found to be about 1e11 cm^{-2} and negative. Published values of generation lifetimes and carrier mobilities are comparable to bulk material and are listed in Table II. Metal-oxide-semiconductor field effect transistors (MOSFETs) made in bonded SOI had generally better subthreshold slopes and leakage currents than bulk devices. Channel carrier mobilities for SOI and bulk devices are comparable. Table III summarizes n- and p-MOS transistor parameters reported by several workers for bonded SOI materials. We measured a lateral diode ideality factor of $n = 1.04$ for a 90 nm thick Si film (10). Krull *et al.* (37) reported $n = 1.15$ for a 2 μm thick Si film. The high-temperature (≈500°C) operation of ring oscillators has been achieved (10). As the above results indicate, the bonded SOI wafer technology produces top-quality devices, in many aspects surpassing other competing technologies. The excellent microscopic properties of the wafers extend beyond single transistors and simple circuits, as demonstrated by recently reported working 256k SRAMs fabricated in a 0.3 μm Si film on SOI substrate (11).

Heterostructures by Wafer Bonding

Wafer bonding techniques can be used to form other semiconductor-on-insulator wafers, where a film of single-crystal semiconductor is formed on a different substrate with an insulating layer between them. A variety of substrate-film combinations allow the use of two different semiconductor material side by side, *e.g.*, InP and Si for optoelectronics with a silicon "brain." The substrate can also be utilized in a passive manner, *e.g.*, a Si wafer providing a mechanical support for brittle GaAs, or a fused quartz substrate allowing optical access to the back of the silicon device layer for optical imaging applications. Successful bonding of GaAs to Si, InP to Si, Ge to Si, and Si to fused quartz, and subsequent thinning, has been demonstrated (39). In some cases, adhesion promoters such as reactively sputter-deposited SiO_2 layers were used. The bonding was performed at temperatures low enough to avoid any failure due to the mismatch of thermal expansion coefficients, yet the bond strength was sufficient to survive the thinning process. The thinning process, augmented by the etching of a stress-relieving pattern, allowed the thermally mismatched films to withstand subsequent device processing temperatures. High electron mobility transistor (HEMT) devices fabricated on thinned GaAs and InP bonded to silicon show no deterioration of their electrical parameters in comparison with similar devices formed on bulk substrates (39).

Conclusions

The wafer bonding technique offers a wide range of choices for the thicknesses of the silicon and insulating oxide films. Oxide thicknesses ranging from zero, for bulk silicon power devices, to full substrate thickness (i.e., a fused quartz wafer) for microwave and optoelectronic applications are available. Both silicon and oxide films retain the structural and electrical quality of bulk material and remain superior to that of other SOI materials. Si films can be as thin as 30 nm for fully depleted MOSFETs with high transient radiation hardness, high-temperature performances and high speed, and as thick as tens or hundreds of micrometers for high-power, high-voltage SOI circuits.

Table III. MOS device parameters comparison for the wafer-bonding SOI and bulk silicon substrate

N-MOS			P-MOS			Silicon film thickness (μm)	References
Mobility [cm²/Vs]	Subthreshold slope (mV/dec)	Leakage current (pA/μm)	Mobility [cm²/Vs]	Subthreshold slope (mV/dec)	Leakage current (pA/μm)		
640	140[a]	0.05				1.3	Spangler and Wise (35)
	68	<0.1		68	<0.1	0.02-0.1	Maszara *et al.* (10)
451	65[a]	<0.001	179	100[a]	<0.05	0.4	Lasky *et al.* (5)
(454)[b]	(130)[a]	(<0.001)					Lasky *et al.* (5)
590	118	1.0	300	90	0.2	0.5	Palkuti *et al.* (36)
(610)	(112)	(0.8)	(310)	(80)	(0.2)		Palkuti *et al.* (36)
451			124			2.0	Krull *et al.* (37)
(468)			(151)				Krull *et al.* (37)
	70[a]	<0.1				0.5	Gotou *et al.* (26)
753						0.18	Caviglia (38)

[a] Evaluated from a plot.
[b] Control bulk data in paretheses.

ning are two-pronged. The no-stop polish-back is most promising for thick SOI films (>1 μm) and at this point is near commercialization by one of the major wafer suppliers (40). The etchback of wafers with double-epi layer seems to be the best candidates for thin SOI films (<0.5 μm) for CMOS applications, at least until polishing with small-area tool matures.

Bonded SOI shows excellent electrical performance with film properties comparable to bulk material. All the processing steps lend themselves to automation and/or batch processing and are highly compatible with the bulk wafer production environment, particularly the polish-back techniques.

Bonding techniques also bring the promise of expansion of the standard SOI structure into a broader spectrum of semiconducting and insulating materials combined on a single wafer.

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REFERENCES

1. D. M. Kenney, U.S. Pat. 3,332,137 (1967).
2. G. Wallis and D. I. Pomerantz, *J. Appl. Phys.*, 40, 3946 (1969).
3. T. R. Anthony, *ibid.*, 58, 1240 (1985).
4. R. C. Frye, J. E. Griffith, and Y. H. Wong, *This Journal*, 133, 1673 (1986).
5. J. B. Lasky, S. R. Stiffler, F. R. White, and J. R. Abernathey, *IEDM Tech. Dig.*, 684 (1985).
6. J. B. Lasky, *Appl. Phys. Lett.*, 48, 78 (1986).
7. M. Shimbo, K. Furukawa, F. Fukuda, and K. Tanzawa, *J. Appl. Phys.*, 60, 2987 (1986).
8. K. Petersen, P. Barth, J. Poydock, J. Brown, J. Mallon, and J. Bryzek, *Solid State Sensor and Actuator Workshop, Tech. Dig.*, 144 (1988).
9. H. Ohashi, J. Ohura, T. Tsukakoshi, and M. Simbo, *IEDM Tech. Dig.*, 210 (1986).
10. W. P. Maszara, G. Goetz, A. Caviglia, and J. B. McKitterick, *J. Appl. Phys.*, 64, 4943 (1988).
11. H. Gotou, A. Sekiyama, T. Seki, S. Nagai, N. Suzuki, M. Hayasaka, Y. Matsukawa, M. Miyazima, Y. Kobayashi, S. Enomoto, and K. Imaoka, *IEDM Tech. Dig.*, 912 (1989).
12. W. Maszara, G. Goetz, T. Caviglia, A. Cserhati, G. Johnson, and J. B. McKitterick, *Mat. Res. Soc. Symp. Proc.*, 107, 489 (1988).
13. J. A. E. Taylor, J. A. Hockey, and B. Pethica, *Proc. Brit. Ceram. Soc.*, 5, 133 (1965).
14. R. Stengl, T. Tan, and U. Gosele, *Jpn. J. Appl. Phys.*, 28, 1735 (1989).
15. X.-L. Xu and Q.-Y. Tong, *Electron. Lett.*, 25(6), 394 (1989).
16. X.-L. Xu, J. Zhan, H. Shen, and Q.-Y. Tong, Extended Abstracts of the 20th Conference on Solid State Devices and Materials, Tokyo, 197 (1988).
17. R. Stengl, K.-Y. Ahn, and U. Gosele, *Jpn. J. Appl. Phys.*, 27, L2364 (1988).
18. J. Haisma, G. A. C. Spierings, U. K. P. Biermann, and J. A. Pals, *ibid.*, 28, 1426 (1989).
19. C. Harendt, W. Appel, H.-G. Graf, B. Hofflinger, and E. Penteker, *This Journal*, 136, 3547 (1989).
20. P. O. Hahn, I. Lampert, and Schnegg, *Proc. Mat. Res. Soc. Symp.*, 105 (1988).
21. R. D. Black, E. L. Hall, N. Lewis, R. S. Gilmore, S. D. Arthur, and R. D. Lillquist, *ibid.*, 107, 495 (1988).
22. S. Bengtsson and O. Engstrom, *This Journal*, 137, 2297 (1990).
23. V. Lehmann, U. Goesele, and K. Mitani, *Solid-State Technol.*, 33, 91 (1990).
24. G. Goetz, Private communication.
25. Y. Arimoto, H. Gotou, K. Ueno, K. Imaoka, and M. Ozeki, 46th Annual Device Research Conference IEEE, Boulder, CO, June 1988.
26. H. Gotou, Y. Arimoto, M. Ozeki, and K. Imaoka, *Fujitsu Sci. Tech. J.*, 24, 408 (1988).
27. J. Haisma, T. M. Michielsen, and G. A. C. M. Spierings, *Jpn. J. Appl. Phys.*, 28, L725 (1989).
28. T. Matsushita, H. Satoh, M. Shimanoe, A. Nieda, A. Ogasawara, M. Yamagishi, and A. Yagi, 47th Annual Device Research Conference IEEE, Cambridge, MA, June 1989.
29. A. Yamada, O. Okabayashi, T. Nakamura, E. Kanda, and M. Kawashima, 5th International Workshop on Future Electron Devices—3D Integration, Miyagi-Zao, May-June 1988.
30. H. Muraoka, T. Ohhashi, and Y. Sumitomo, in "Semiconductor Silicon 1973," H. R. Huff and R. R. Burgess, Editors, p. 327, The Electrochemical Society Softbound Proceedings Series, Princeton, NJ (1973).
31. N. F. Raley, Y. Sugiyama, and T. Van Duzer, *This Journal*, 131, 161 (1984).
32. A. Soderbarg, IEEE SOS/SOI Technology Conference, Stateline, NV, Oct. 1989.
33. V. Lehmann, Paper 306 presented at The Electrochemical Society Meeting, Montreal, Quebec, Canada, May 6-11, 1990.
34. D. Godbey, H. Hughes, F. Kub, M. Twigg, L. Palkuti, P. Leonov, and J. Wang, IEEE SOS/SOI Technology Conference, Stateline, NV, Oct. 1989.
35. L. J. Spangler and K. D. Wise, *IEEE Electron Dev. Lett.*, EDL-8, 137 (1987).
36. L. J. Palkuti, P. Ling, P. Leonov, H. Kawayoshi, R. Ormond, and J. Yuan, *IEEE Trans. Nucl. Sci.*, 35, 1653 (1988).
37. W. A. Krull, J. F. Buller, G. V. Rouse, and R. D. Cherne, *IEEE Circuits Devices Mag.*, p. 20, July 1987.
38. A. Caviglia, Unpublished.
39. G. Goetz and A. Fathimulla, IEEE SOS/SOI Technology Conference, Stateline, NV, Oct. 1989.
40. T. Abe, Private communication.